

REMARKS/ARGUMENTS

Claims 1, 4-43 remain pending and claims 2 and 3 have been canceled without prejudice. Claims 1, 18 and 31 have been amended, as recited hereinabove.

Claims 1, 6-14, 18-19, 23-32 and 36-43 have been rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Grieff et al. (US Patent No. 6,961,813) (hereinafter "Grieff") in view of "SATA vs. PATA: The Reality of Serial and Parallel ATA – Serial ATA" and further in view of Talati (US Patent No. 6,763,402) (hereinafter "Talati"). It is believed however that the foregoing amended claims, as recited hereinabove, are patentable and all claims depending therefrom are patentable over Grieff in view of "SATA vs. PATA: The Reality of Serial and Parallel ATA – Serial ATA" and further in view of Talati.

In the claimed invention, the first and second task files are each separately responsive to commands from the first and second host units, respectively, and as such they allow for "concurrently accessing the device, through the switch, by accepting commands, from either of the first or second host units, at any given time, ...". Furthermore, arbitration is not performed until after commands have been stored in the task files. In contrast thereto, Talati uses a single queue, i.e. buffer RAM 194 and performs arbitration of commands prior to queuing, which are some of the reasons, among others, for preventing Talati from "accepting commands, from either host, at any given time". [See Talati: Col. 5, lns. 26-30].

Moreover, the combination of Grieff and Talati is believed to be erroneous as Talati is directed to the problem of interfacing a data storage device, a SATA device, to a plurality of host data processing systems, through an IEEE 1349a bus and therefore uses bridges to convert the interface protocols and, whereas, Grieff is directed to a switch receiving input, through SATA ports, from multiple host devices and an arbiter module for assigning a priority scheme to received commands and for transmission thereof to a storage device through SATA ports. Therefore, Talati would not have been motivated to solve the problem solved by the claimed invention by using the teachings of Grieff, as Talati did not consider receiving input from SATA ports.

It is therefore believed that claims 1, 18 and 31 are patentable over Grieff in view of "SATA vs. PATA: The Reality of Serial and Parallel ATA – Serial ATA" and further in view of Talati and all claims depending therefrom are also necessarily patentable.

Claims 2-4, 20-22 and 33-35 have been rejected under 35 U.S.C. 103(a) as being allegedly unpatentable over Grieff, "SATA vs. PATA: The Reality of Serial and Parallel ATA – Serial ATA" and Talati and further in view of Ng (US Patent No. 6,388,590) (hereinafter referred to as "Ng").

It is believed that Ng also lacks separate task files for each host and therefore does not render the claimed invention obvious in combination with the foregoing references. For example, in Fig. 3, if the PC 52 is perceived as a host, there is only one task file 72b in the CD-ROM device 54. Furthermore, there is only one host and arbitration is not done after receipt of commands. Therefore, it is believed that the claimed invention is patentable over Grieff, "SATA vs. PATA: The Reality of Serial and Parallel ATA – Serial ATA" and Talati and further in view of Ng.

Claim 5 has been rejected under 35 U.S.C. 103(a) as being unpatentable over Grieff, "SATA vs. PATA: The Reality of Serial and Parallel ATA – Serial ATA", Talati and Ng and further in view of Boucher et al. (US Patent No. 6,434,620) (hereinafter referred to as "Boucher"). For the foregoing reasons, among others, it is believed that claim 5 is patentable over Grieff, "SATA vs. PATA: The Reality of Serial and Parallel ATA – Serial ATA", Talati and Ng further in view of Boucher.

Claims 15-16 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Grieff, "SATA vs. PATA: The Reality of Serial and Parallel ATA – Serial ATA", and Talati and further in view of "Serial ATA Specification". For the foregoing reasons, among others, it is believed that claims 15 – 16 are patentable over Grieff, "SATA vs. PATA: The Reality of Serial and Parallel ATA – Serial ATA", and Talati and further in view of "Serial ATA Specification".


Claim 17 has been rejected under 35 U.S.C. 103(a) as being unpatentable over Grieff, "SATA vs. PATA: The Reality of Serial and Parallel ATA – Serial ATA", and Talati and further in view of Boucher. For the foregoing reasons, among others, it is believed that claim 17 is patentable over Grieff, "SATA vs. PATA: The Reality of Serial and Parallel ATA – Serial ATA", and Talati and further in view of Boucher.

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Reconsideration and allowance of claims 1, 4-43 is hereby respectfully requested. Applicants submit that the subject application is now in condition for allowance and an early notice thereof is respectfully requested. Should any further amendment be required prior to passing the application to issue, the Examiner is respectfully invited to contact the undersigned by telephone at the number set out below.

Respectfully submitted,
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I hereby certify that this correspondence with all attachments is being deposited with the U.S. Postal Service as first class mail in an envelope addressed to: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria VA 22313-1450 on November 6, 2006 by Erika Villafana.

